OPERATOR'S MANUAL

CAPACITANCE CONDUCTANCE METER

Model 72 BC

MATERIALS DEVELOPMENT CORPORATION

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MP MASTER

MA24741

This manual describes the Materials Development proprietary modification to the Boonton Model 72B 1 MHz capacitance meter which gives the instrument the added capability of measuring the loss component (or conductance) of the device under test (usually a capacitor).

In addition to the standard analog output of capacitance, the MDC modification provides a second analog output voltage which is proportional to the equivalent parallel conductance of the device under test. The front panel meter can be switch selected to indicate either the equivalent parallel capacitance (in units of picofarads) of the device under test or the equivalent parallel conductance (in units of 2 pi microsiemens). That is, the panel meter and the analog output voltages are scaled to indicate parallel conductance in units of an equivalent capacitance:

$$G_{peq}\ (\mu S) = 2\ \pi\ C_{peq}\ (pF)$$

where Cpeq (pF) can be read directly from the panel meters or by way of measuring the analog output voltage of the conductance channel.

The modified instrument retains all of its original, standard capacitance measurement capabilities and specifications. The modified instrument measures the equivalent parallel conductance of the device under test on each of the instrument's original ranges. No new ranges are added and the conductance ranges are not independently selectable.

The standard capacitance ranges are listed below along with their accompanying conductance ranges. It should be understood from the above that when a capacitance range is selected, the accompanying conductance range is also selected by default.

Equivalent Parallel Capacitance (pF)/FS	Equivalent Parallel Conductance (μS)FS	Equivalent Parallel Resistance (Ω)FS
0 to 3.000	0 to 18.850	∞ to 53000.
0 to 30.00	0 to 188.50	∞ to 5300.0
0 to 300.0	0 to 1885.0	∞ to 530.00
0 to 3000.	0 to 18850	∞ to 53.000

It should be noted that the full scale values of resistances are minimums while the full scale values of capacitances and conductances are maximums.

Conductance Channel Specifications (72BC)

dc Output:	For $Q \leq 0.2$
- Level:	3.0 volts FS for all ranges.
- Linearity:	±(0.1% of reading = 0.01% of FS).
	±(0.25% of reading = 0.01% of FS) on the 18850 μS (3000 pF) range.
- Response Time:	1 m sec
-Source Resitance	1 Kilo ohm

Only the 3-series ranges are mentioned above for the model 72B since the 1-series ranges merely apply to the front panel meter scale.

I. PRINCIPLE OF OPERATION

A. THE STANDARD INSTRUMENT

The overall principle of operation of the Boonton model 72 series capacitance meters is illustrated by the simplified schematic shown in Figure 1.

The 1 MHz oscillator serves as a small-signal voltage source and generates a 15 millivolt (RMS) sinusoid at the LO-TEST terminal. An identical but apposite (180° out of phase) sinusoid is generated at the LO-DIFF terminal.

The device under test is connected between the LO and HI-TEST terminals (or the LO and HI-DIFF terminals). The HI terminals are common and are connected to one of three series resonant LC networks (RANGE NETWORKS in Figure 1) which simultaneously present a very low impedance to ground and perform a current to voltage conversion. Therefore, the HI side of the device under test is (for practical purposes) connected to an ac ground while the 1 MHz current which flows through the device under test is converted to a voltage across the capacitor of the series-resonant LC range network.

This voltage is subsequently amplified by a high gain, tuned (1 MHz) amplifier and used to drive a balanced synchronous detector.

The 1 MHz oscillator also generates a reference sinusoid which is phase shifted 90° from the voltage present at the LO-TEST terminal, amplified (to approximately 10 volts) and used to (over) drive the other side of the synchronous detector. The output of the synchronous detector is a dc voltage (positive or

negative) which is proportional to the amplitude of the current component flowing through the device under test, which is 90° out of phase with the voltage across the device under test. Thus, the dc voltage output of the synchronous detector is proportional to the equivalent parallel capacitance (or inductance) of the device under test at a frequency of 1 MHz. The detector output is buffered and scaled by the output operational amplifier (op-amp) so as to provide a full scale voltage of 3 volts for the 3-series ranges. The 1-series ranges are derived by merely switching the attenuation of the front panel meter.

Both the out of phase (±90°) current component and the in phase (0°) current component of the device under test are processed up to the syncronous detector. Therefore these instruments can be modified to provide a capability for measuring the loss component (or equivalent parallel conductance) of the device under test by merely adding a second channel which detects the amplitude of the current component through the device under test which is in phase with the voltage across the device under test. The MDC conductance modification implements such a capability.

B. THE MDC MODIFIED INSTRUMENT

The overall principal of operation of the Boonton model 72BC capacitance meter with the MDC conductance modification included is illustrated by the simplified schematic shown in Figure 2.

A second (identical) high gain, tuned amplifier is added with its input connected in parallel with the original tuned amplifier. The output of the second amplifier drives a second (identical) synchronous detector. The reference sinusoid from the 1 MHz oscillator is phase shifted by 90°, amplified, and used to (over) drive the other side of the second synchronous detector. The output of the second synchronous detector is a dc voltage (positive or negative) which is proportional to the amplitude of the current component through the device under test which is in phase with the voltage across the device under test. Thus the dc output voltage of the second synchronous detector is proportional to the equivalent parallel conductance of the device under test at a frequency of 1 MHz.

The output of the second detector is buffered and scaled by a second output op-amp to provide a full scale voltage of 3 volts for the 3-series ranges.

The MDC-added second amplifier, detector, and op-amp are hereafter referred to as the conductance channel while the original amplifier, detector, and op-amp are referred to as the capacitance channel.

The front panel meter is switched between the output of the op-amps of the capacitance and conductance channels. Analog output voltages are simultaneously available from both the capacitance and conductance channel in the 72B.

II. CALIBRATION PROCEDURE

This section includes calibration procedures for:

1. The standard capacitance function (hereafter referred to as the capacitance channel) of the Boonton model 72 capacitance meter, and
2. The conductance channel on those instruments which have received the MDC modification which adds a conductance measurement capability to these instruments.

Emphasis is placed upon the calibration of the complete analog signal paths of the 72B by making use of the analog outputs of the instruments. The calibrations of the panel meter can be treated independently of the overall calibration of the analog signal paths.

Before starting the calibration procedure:

- Turn power off.
- Install covers with access holes for all calibration adjustments.
- Install the model 72-4B input fixture.
- Mechanically zero the panel meter on the 72B
- Turn power on to:
  - The 72BC
  - A 4-1/2 digit DVM.
  - An oscilloscope with a bandwidth of at least 10 MHz and a minimum deflection factor of 5 mv/div with a minimum input impedance of 1 Megohm.
- Wait one hour to begin the calibration procedure.

The following items are required for the calibration:

- Standard capacitances for each range.
- Standard conductances for each range.
- A 500 pF loading capacitor with a male BNC connector.
- A 200 pF loading capacitor with a male BNC connector.
- A HI-Q/LO-Q test fixture with a nominal capacitance of 100 pF. (Described in the Boonton 72B manual.)
- Insulated tuning tools.

The calibration should be performed at the same temperature at which the instrument will be used for making measurements.

The test point and adjustment locations are shown in Figure 3.

III. THE CAPACITANCE CHANNEL

The calibration of the capacitance channel is independent of the calibration of the conductance channel. However, if the instrument is to include the MDC conductance channel, then the conductance channel hardware must be installed and completely functional during the calibration of the capacitance channel.

1. - Remove the top cover.
2. - Connect the LO side of DVM to the ground banana jack on the rear of the instrument.
   - Connect the HI side of the DVM to the +15 volt supply.
   - Adjust R115 to obtain +15.00 volts.
3. - Connect the HI side of the DVM to the -15 volt supply.
   - Adjust R118 to obtain -15.00 volts
4. - Connect the LO side of the DVM to TP2 and ground TP2.
   - Connect the HI side of the DVM to the analog output banana jack on the rear of the instrument.

- Adjust R133 to obtain 0.000 volts offset for the output op-amp.
- Disconnect the DVM.

5. - Connect the LO side of the DVM to ground.
   - Connect the HI side of the DVM to TP1.
   - Adjust C202 to obtain a maximum dc voltage on TP1. If the maximum is not at least 7.5 volts, the oscillator/amplifier board will need a modification.
   - Disconnect the DVM.
6. - Connect the LO side of the oscilloscope's vertical input amplifier to ground.
   - Connect the HI side of the oscilloscope's vertical input amplifier to the TEST-LO BNC input connector on the front panel.
   - Adjust the horizontal sweep of the oscilloscope to permit viewing a 1.0 MHz sinusoid.
   - Adjust R202 to obtain approximately 15 mv RMS (42.42 mv peak-to-peak).
7. - Connect the HI side of the oscilloscope's vertical input amplifier to TP3.
   - Select the 30pF range.
   - Adjust the front panel capacitance zero control to obtain approximately 40 mv peak-to-peak.
   - Adjust C233 to obtain the best sinusoidally shaped waveform.
   - Disconnect the oscilloscope.

8. - Install the top cover with adjustment access holes and wait at least 15 minutes.

9. - Connect the LO side of the DVM to ground.
   - Connect the HI side of the DVM to the analog output.
   - Select the 3 pF range.
   - Adjust the front panel capacitance zero control to obtain 0.000 volts...hereafter referred to as zeroing the capacitance channel.

10. - Select the 3000 pF range.
    - Adjust R242 to obtain 0.000 volts.

11. - Iterate steps 9 and 10 until 0.000 volts is obtained on both the 3 pF and 3000 pF ranges without the need for adjustments.

12. - Select the 300 pF range.
    - Zero the capacitance channel.
    - Install the HI-Q/LO-Q test fixture on the input TEST terminals.
    - Adjust C228 to obtain identical output voltages for both the HI-Q and LO-Q conditions. If orthogonality cannot be obtained, it may be necessary to add a small capacitor in parallel with C228.
    - Remove the HI-Q/LO-Q test fixture.

13. - Select the 300 pF range.
    - Zero the capacitance meter.
    - Install a standard capacitor on the input TEST terminals using "TEE" BNC connectors.

- Adjust R144 to obtain the current output voltage. NOTE: The full scale output voltage is 3.000 volts for 300 pF
- Remove the standard capacitor.

14. - Install a 500 pF loading capacitor between the TEST-HI input terminal and ground.
- Zero the capacitance channel.
- Install the standard capacitor as was used in step 13 on the input TEST terminals.
- Adjust L104 to obtain the correct output voltage.
- Remove the standard capacitor and the loading capacitor.

15.- Iterate steps 13 and 14 until identical output voltages are obtained with and without the loading capacitor. If identical output voltages cannot be obtained, one of the fixed-value components in the 300 pF range's input network will need replacement with a different value.

16.- Select the 3000 pF range.
- Zero the capacitance channel.
- Install a standard capacitor on the input TEST terminals.
- Adjust C121 to obtain the correct output voltage.
- Remove the standard capacitor.

17.- Select the 30 pF range.
- Zero the capacitance channel.
- Install a standard capacitor on the input TEST terminals using "TEE" BNC connector.
- Adjust C117 to obtain the correct output voltage.
- Remove the standard capacitor.

18. - Install a 500 pF loading capacitor between the TEST-HI input terminal and ground.
- Zero the capacitance channel.
- Install the same standard capacitor which was used--Step 17.
- Adjust L103 to obtain the correct output voltage.
- Remove the standard capacitor and loading capacitor.

19. - Iterate steps 17 and 18 until identical output voltages are obtained with and without the loading capacitor. If output voltages cannot be obtained, one of the fixed-value components in the 30 pF range's input network will need replacement with a different value.

20. - Select the 3 pF range.
- Zero the capacitance channel.
- Install a standard capacitor on the input TEST terminals using "TEE" BNC connectors.
- Adjust C111 to obtain the correct output voltage.
- Remove the standard capacitor.

21. - Install a 200 pF loading capacitor between the TEST-HI input terminal and ground.
- Zero the capacitance channel.
- Install the same capacitor as was used in step 20 on the input TEST terminals.
- Adjust L102 to obtain the correct output voltage.
- Remove the standard capacitor and the loading capacitor.

22. - Iterate steps 20 and 21 until identical output voltages are obtained with and without the loading capacitor. If identical output voltages cannot be obtained, one of the fixed-value components in the pF range's input network will need replacement with a different value.
    - Remove the "TEE" BNC connectors.

23. - Select the 300 pF range.
    - Zero the capacitance channel...must be precise.
    - Install a standard capacitor on the input TEST terminals.
    - Record the output voltage.
    - Remove the standard capacitor.

24. - Install the same standard capacitor as was used in step 23 on the input DIFF terminals.
    - Record the output voltage...will be negative.
    - Remove the standard capacitor.

25. - Iterate steps 23 and 24 while adjusting T401CT to obtain identical magnitudes for the output voltages when the standard capacitor is installed on either the TEST or DIFF input terminals.

26. - Repeat steps: 13, 14, and 15.
    - If L104 required adjustment when steps 13, 14, and 15 were repeated, then repeat steps: - 17 through 22.

27. - Do not adjust L201 and T201 unless the instrument cannot be calibrated to meet the specifications.

- If L201 and or T201 need adjustments, follow the procedure in the Boonton manual and then repeat the entire above calibration procedure.

28. - Some of the above adjustments are slightly interactive. Therefore, if ultimate precision is required, the entire calibration procedure should be repeated. One repeat is adequate.

- Note that if the temperature of the instrument drifts by as much as one or two degrees Celsius, the calibration will appear to be in error.

29. - Front panel meter calibration:

A.- Select the 300 pF range.

- Zero the capacitance channel.
- Install a standard capacitor on the input TEST terminals
- Adjust R146 to obtain the correct panel meter indication.
- Remove the standard capacitor.

B.- Select the 100 pF range.

-Zero the capacitance channel.

-Install a standard capacitor on the input TEST terminals.

-Adjust R142 to obtain the correct panel meter indication.

-Remove the standard capacitor.

IV. THE CONDUCTANCE CHANNEL

The calibration of the conductance channel must be performed after the calibration of the capacitance channel has been completed.

The calibration of the conductance channel is, in principle, similar to the calibration of the capacitance channel. However, there are a few fundamental differences.

A. A 90° phase shift network is used to obtain the reference sinusoid for the conductance channel. Therefore, the phase shift adjustment replaces the oscillator adjustment.

B. The gains of the individual conductance ranges are not separately adjustable. Only one of the ranges can have its analog output voltage adjusted to exactly the correct value. All other ranges will be in error by a small amount and their output voltages must be multiplied by a calibration factor which is calculated and which is different for each range, but very near unity for all ranges.

C. No loading compensation adjustments are necessary. The loading adjustments performed during the calibration of the capacitance channel also serve the conductance channel.

D. The calibration is carried out in terms of equivalent capacitances.

1. - Remove the top cover.

2. - Connect the LO side of the DVM to TP2 on the conductance channel oscillator/amplifier board and ground TP2.

   - Connect the HI side of the DVM to the analog output of the conductance channel.

- Adjust the offset of the conductance channel output op-amp to obtain 0.000 volts.
- Disconnect the DVM.

3. - Connect the LO side of the oscilloscope's vertical input amplifier to ground.
   - Connect the HI side of the oscilloscope's vertical input amplifier to TP3 on the conductance channel oscillator/amplifier board.
   - Select the 30 pF range.
   - Adjust the front panel conductance zero control to obtain approximately 40 mv peak-to-peak.
   - Adjust C233 on the conductance channel oscillator/amplifier board to obtain the best sinusiodally shaped waveform.
   - Disconnect the oscilloscope.
4. - Reinstall the top cover with adjustment access holes.
5. - Connect the LO side of the DVM to the analog output of the conductance channel.
   - Select the 3 pF range.
   - Adjust the front panel conductance zero control to obtain 0.000 volts...hereafter referred to as zeroing the conductance channel.
6. - Select the 3000 pF range.
   - Adjust R242 on the conductance channel oscillator/amplifier board to obtain 0.000 volts.

7. - Iterate steps 5 and 6 until 0.000 volts is obtained on both the 3 pF and 3000 pF ranges without the need for adjustments.

8. - Select the 300 pF range.
   - Zero the conductance channel.
   - Install a standard conductor on the input TEST terminals using "TEE" BNC connectors.
   - Adjust the gain of the conductance channel output op-amp to obtain the correct panel meter indication:
     $Ceq = G/2\pi f = G/2\pi E6$.
   - Adjust the conductance channel output level to obtain the correct output voltage for the equivalent capacitance:
     $Ceq = G/2\pi E6$ and the full scale output voltage is 3 volts for the 300 pF range.

9. - Install a standard capacitor (of such value that the resultant Q of the parallel G-C combination is approximately 1/3) in parallel with the standard conductor.
   - Adjust the 90° phase shift capacitor and/or C228 on the conductance channel oscillator/amplifier board to obtain the correct ouput voltage. The conductance of the added standard capacitor must be taken into account.
   - Remove the standard capacitor.

10. - Iterate steps 8 and 9 until the correct panel meter indications and output voltages are obtained with and without the added standard capacitor. When the added

capacitor is in place, the output voltage should be larger by an amount corresponding to the conductance of the standard capacitor. If orthogonality cannot be obtained, it may be necessary to add a small capacitor in parallel with either the 90° phase shift capacitor or C228 on the conductance channel oscillator/amplifier board.

- Remove the standard capacitor and the standard conductor.

11. - Do not adjust L201 and T201 on the conductance channel oscillator/amplifier board unless the instrument cannot by calibrated to meet the specifications. If L201 and/or T201 need adjustment, follow the procedure in the Boonton manual and then repeat the entire above calibration procedure for the conductance channel.

There are no further adjustments which can be made for the calibration of the conductance channel. Further calibration of the individual conductance ranges requires the measurement of a standard conductor on each range and the calculation of a calibration "GAIN FACTOR" (GF) for each range, which is subsequently applied to all measurements made with the conductance channnel. The front panel conductance zero control permits manual zeroing and therefore no calibration "OFFSET FACTORS" need be calculated for manual use of the instrument. However, the calculation and application of both OFFSET and GAIN factors for both the capacitance channel and the conductance channel are recommended for situations where the instrument is to be used in a computer controlled system. The use of OFFSET factors is necessary when manual zeroing cannot be performed.

The calculation of the conductance channel gain factors is outlined below:

- Select the range of interest.
- Zero the conductance channel.
- Install a standard conductor on the input TEST terminals.
- Record the output voltage.
- Calculate the gain factor:

  GF(x) = (standard G value)/(measured G value)

  x= 3, 30, 300, 3000 pF range.

Subsequently, when an unknown conductance is to be measured, the corrected value of conductance is obtained from:

Gunknown = GF(x) * measured conductance value.

12. - Turn power off.
    - Remove the calibration covers and install the original covers.
13. - Drifts due to temperature changes are best corrected by adjustmemt of R202.

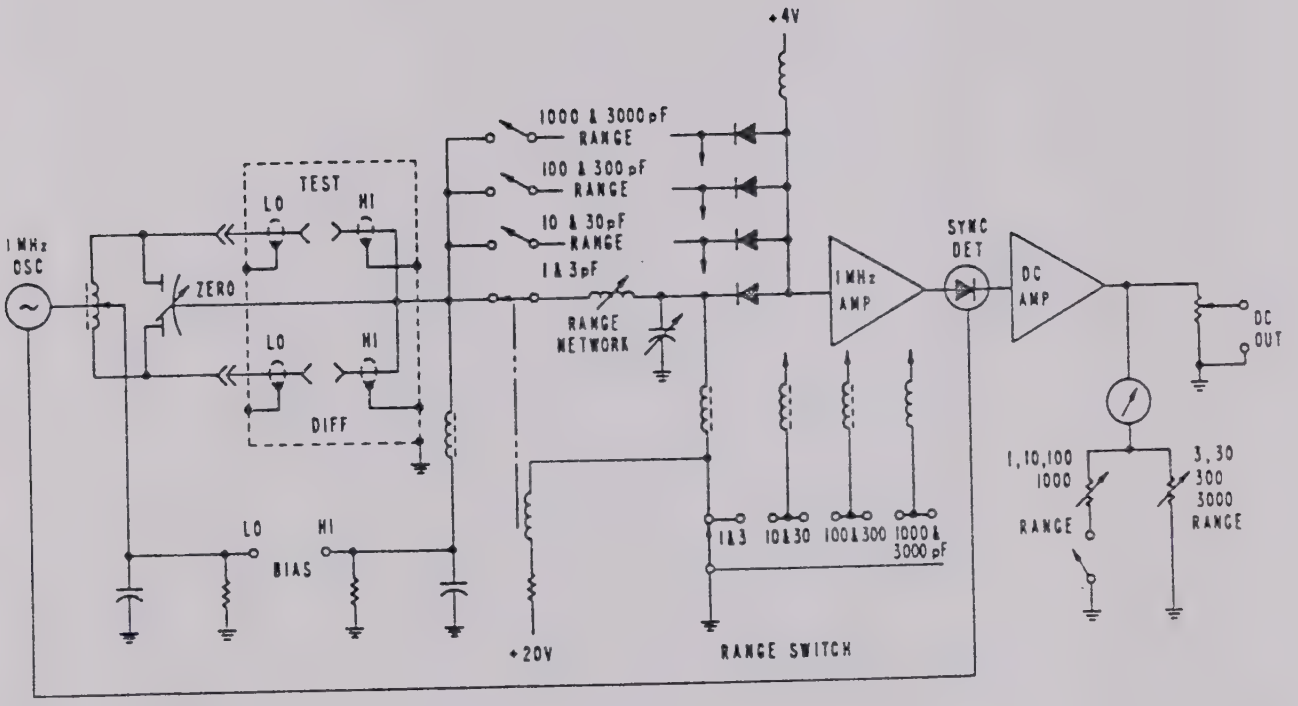
+4V
1000 & 3000 pF RANGE
100 & 300 pF RANGE
10 & 30 pF RANGE
1 & 3 pF
TEST
LO
HI
ZERO
LO
HI
DIFF
1 MHz OSC
RANGE NETWORK
1 MHz AMP
SYNC DET
DC AMP
DC OUT
1,10,100 1000
RANGE
3,30 300 3000 RANGE
LO
HI
BIAS
1&3
10&30
100&300
1000 & 3000 pF
+20V
RANGE SWITCH

Figure 1

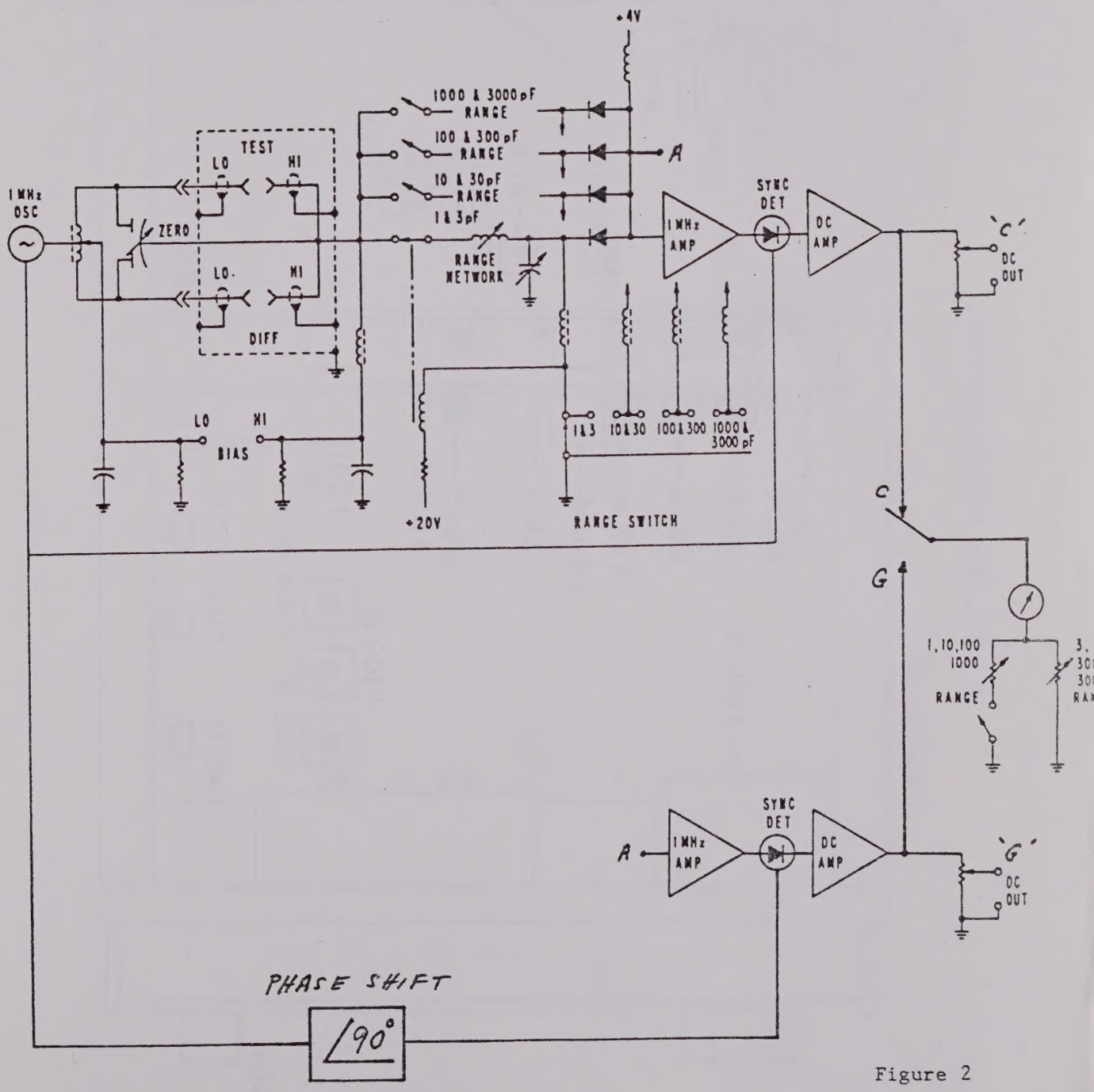
+4V
1000 & 3000 pF RANGE
100 & 300 pF RANGE
10 & 30 pF RANGE
1 & 3 pF
A
TEST
LO
HI
ZERO
LO.
HI
DIFF
1 MHz OSC
RANGE NETWORK
1 MHz AMP
SYNC DET
DC AMP
'C'
DC OUT
LO
HI
BIAS
+20V
1 & 3
10 & 30
100 & 300
1000 & 3000 pF
RANGE SWITCH
C
G
1, 10, 100 1000
RANGE
SYNC DET
A
1 MHz AMP
DC AMP
'G'
DC OUT
PHASE SHIFT
90°

Figure 2

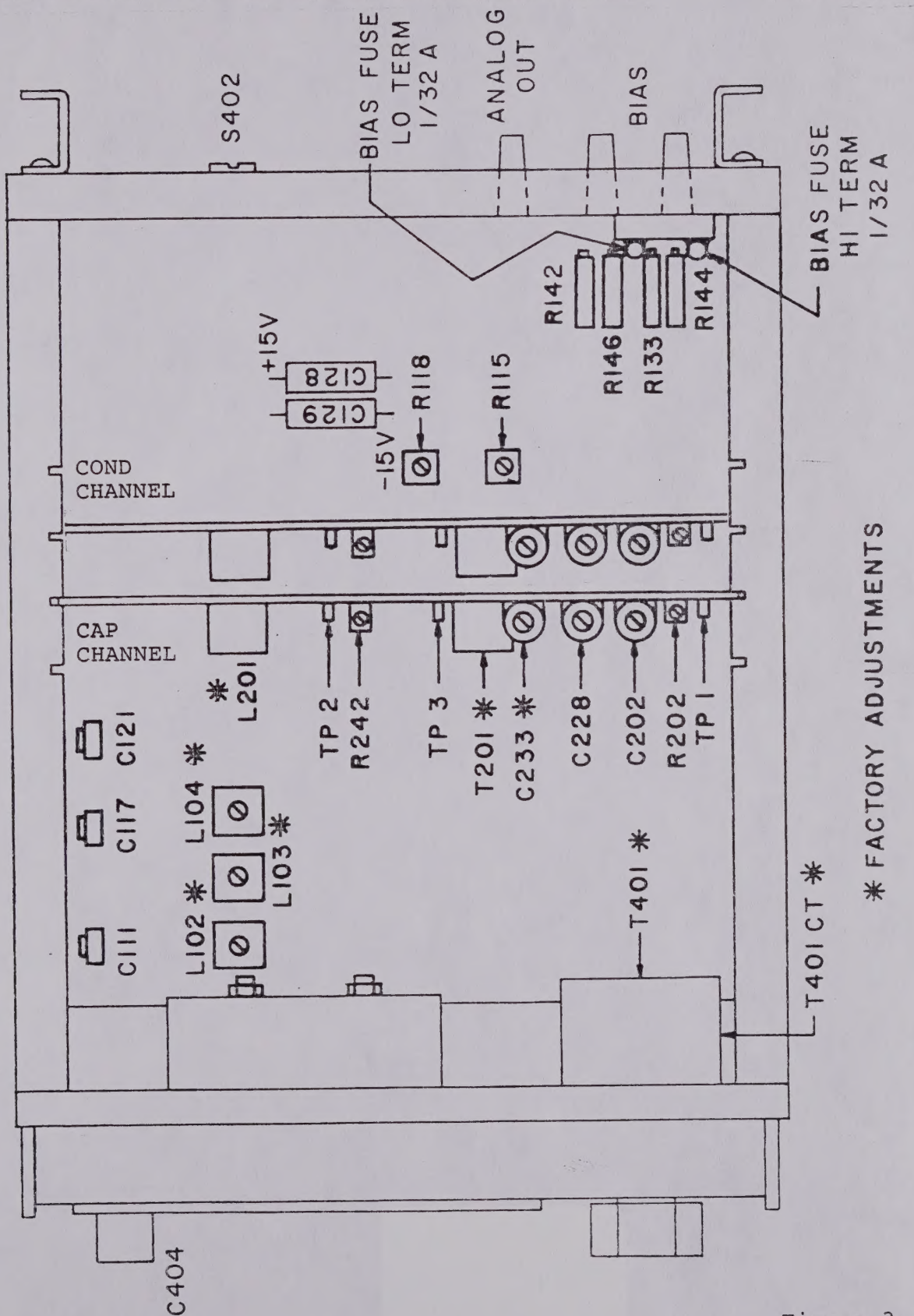
S402
BIAS FUSE LO TERM 1/32 A
ANALOG OUT
BIAS
BIAS FUSE HI TERM 1/32 A
R142
R146
R133
R144
+15V
C128
C129
-15V
R118
R115
COND CHANNEL
CAP CHANNEL
L201 *
TP 2
R242
TP 3
T201 *
C233 *
C228
C202
R202
TP 1
C121
C117
C111
L104 *
L103 *
L102 *
T401 *
T401 CT *
C404
* FACTORY ADJUSTMENTS

Figure 3.

ADC PORTION

WHAT ABOUT THE AVERAGES

CURRENT MONITOR CHECK

"BART" "MARK"

818-700-8290

4607

JOHN. ROZNOVSKY

2213-41

BUNO

RMA
0512884

$75.00
4
300.00

POT = 100K

72BC

0621008345

17HK
17HK

21541 NORDHOFF ST
UNIT B
CHATSWORTH, CALIF.
91311

MP MASTER
MA24741